WHAT IS CLAIMED IS:

1. An error correction device comprising: a buffer memory for storing at least one sector of data having a structure where each of N words of error correcting code comprises a data unit, an inner code parity unit, and one error detecting code; a syndrome calculating means for generating syndrome for data read from said buffer memory; an error correcting means for correcting error-containing data in said buffer memory by detecting an error position from the syndrome generated by said syndrome calculating means and by calculating an error value; an error detecting means for detecting an error, one sector at a time, in error-corrected data generated by said error correcting means; a storing means for storing mid-term results, in code word units, of an error detecting process in said error detecting means; a bus control means for controlling data transfer between said buffer memory, said syndrome calculating means, said error correcting means, and said error detecting means; and a system control means for performing various processes for error correction in predetermined procedures a necessary number of times, wherein

said bus control means comprises:

a before-syndrome data transfer sub means for transferring data to be corrected from said buffer memory to said syndrome calculating means and to said error detecting means concurrently in code word units until said syndrome calculating means detects an error-containing code;

an after-syndrome data transfer sub means for, when said syndrome calculating means detects an error-containing code, transferring subsequent data in said buffer memory only to said syndrome calculating

means in code word units; and

an error-detecting data transfer sub means for, after said error correcting means corrects an error contained in data in said buffer memory based on the syndrome transmitted by said syndrome calculating means, transferring error-corrected data which include the code word from which the error-containing code has been detected up to and including a final code word from said buffer memory to said error detecting means in code word units for error detection;

said error detecting means comprises:

a parallel process sub means for, until said syndrome calculating means detects an error-containing code, storing the mid-term results of the error detecting process to said storing means in code word units, and executing error detection of a code word transmitted from said buffer memory in parallel with syndrome calculation done by said syndrome calculating means; and

an after-correction error detecting sub means for, after said syndrome calculating means detects an error-containing code, executing error detection for data transferred from said buffer memory after the error correction done by said error correcting means, following a code word which has previous contents before the occurrence of an error and which is already stored in said storing means.

2. The error detection device of claim 1 further comprising a DMA control means for controlling DMA transfer to said buffer memory, wherein

said system control means comprises:

a first DMA transfer sub means for providing said DMA control means with a first DMA transfer instruction indicating that data to be corrected should be transferred from said buffer memory to said syndrome calculating means and to said error detecting means at the start of an error correcting process; and

a second DMA transfer sub means for, after having been informed of completion of error correction by said error correcting means, only when said syndrome calculating means has detected an error-containing code, providing said DMA control means with a second DMA transfer instruction indicating that subsequent data including a code word from which said error-containing code has been detected based on error-containing code word information transmitted by said syndrome calculating means should be transferred from said buffer memory to said error detecting means; and

said DMA control means comprises:

a transfer control sub means for making a request of said bus control means to perform DMA transfer in accordance with the first DMA transfer instruction and the second DMA transfer instruction transmitted by said system control means.

3. An error correction device comprising: a buffer memory for storing at least one sector of data having a structure where each of N words of error correcting code comprises a data unit, an inner code parity unit, and one error detecting code; a syndrome calculating means for generating syndrome for data read from said buffer memory; an error correcting means for correcting error-containing data in said buffer memory by